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Progress and Challenges in Multijunction Solar Cells Utilizing Ternary and Quaternary Semiconductor Alloys

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ABSTRACT: Multijunction solar cells have emerged as a promising approach to overcome the efficiency To bypass this efficiency constraint of single-junction PV cells, a new type of cell has been developed called multijunction PV cells that can absorb multiple portions of the solar spectrum with various semiconductor layers whose bandgaps have been engineered appropriately. In this study, the development and limitations of ternary and quaternary semiconductor alloys for PV applications will be discussed and their focus will be on the heterojunction solar cells based on $CuInTe_2$ (ternary alloy) and Cu_2ZnSnS_4 (quaternary alloy). The devices were fabricated by electrodeposition method, where CdS was used as a buffer layer, and by optimized controlled annealing treatments to achieve the best structural and optoelectronic properties. Among the devices, the device based on $CuInTe_2$ achieved a maximum power conversion efficiency of ~4.13%, Voc of 480 mV, Jsc of 20 mA/cm2 and FF of 43%. The study emphasizes the key advantages of ternary alloys: high optical absorption and relatively easy composition; and quaternary alloys: high compositional flexibility and earth abundant components for low cost PV applications. But both types of materials are hampered by serious problems, including recombination losses, series resistance, interface mismatch, compositional disorder, and secondary phase formation. They can cause severe hindrance for integration in high-efficiency multijunction architectures. The results indicate that there is a need for further advances in the engineering of the interfaces, the reduction of defect densities and the tuning of the band gaps for the realization of efficient and scalable multijunction solar cells using ternary and quaternary semiconductor alloys.

I. INTRODUCTION

Since multi-junction solar cells may exceed the theoretical restrictions on PV efficiency associated with single-junction solar cells, they represent a significant advancement in photovoltaic (PV) technology. These cells achieve a better efficiency of light conversion by combining several semiconductor layers with different bandgaps to absorb a greater variety of sun spectrum wavelengths (Zidani et al., 2025; Hu et al., 2024). The capacity of ternary and quaternary semiconductor alloys to precisely adjust their composition to guarantee superior spectrum matching and seamless device integration is a key component in this progress (Parola et al., 2025; Amrillah et al., 2023).

Quaternary compounds like AlGaAsSb, AlInAsSb, GaInAsSb, and CZTS have improved compositional flexibility and the potential for affordable thin films, while III–V compounds like InGaP and GaAsSb are known for having high crystalline quality and good performance in multi-junctions (Sansom et al., 2021; Kret et al., 2021). However, a number of technical issues, including structural flaws, compositional inhomogeneity, secondary phase development, interface recombination, and voltage losses, all of which restrict device efficiency, make it difficult to successfully apply these materials in real-world applications (Muhamad & Lafta, 2022; Ennouhi, 2025). Therefore, in order to develop the next generation of high efficiency multi-junction solar cells with ternary and quaternary alloy systems, a thorough understanding of material behaviors, device physics, and interface engineering is required.

Research Objectives

1. To study the performance of the multijunction solar cells using ternary and quaternary semiconductor alloys.

2. To assess the pros and cons of $CuInTe_2$ and CZTS material for PV application.

3. To characterize critical issues in alloy based solar cell including recombination loss, compositional disorder and interface instability.

4. To suggest future strategies of improving the efficiency, stability and scalability of multijunction solar-cell technologies.

II. LITERATURE REVIEW

The multi-junction solar cell is an emerging photovoltaic technology that enables efficient use of solar spectrum and overcomes the limitation in inherent efficiency of single-junction (Zidani et al., 2025; Hu et al., 2024).

Device performance is primarily determined by bandgap engineering, lattice matching, and the minimization of optical and recombination losses between subcells. Due to their high crystalline quality and optimized heterostructure design, III–V tandem systems such as InGaP/GaAs have shown record-breaking efficiencies; however, their widespread industrial use is currently limited by their high production costs and challenging epitaxial fabrication (Helmers et al., 2024; Soley et al., 2024)..

To address these problems, ternary and quaternary semiconductor alloys have been the subject of extensive research for next generation of multi-junction cells. In this light, compounds such as $CuInTe_2$ and GaAsSb are currently explored as potential absorber materials due to their high optical absorption properties and tunable electronic properties (Amrillah et al., 2023; Gonzalo Martín et al., 2021).

Other alloys with a higher number of elements, such as Cu_2ZnSnS_4 (CZTS), AlGaAsSb, AlInAsSb and GaInAsSb, have a wider compositional range. This flexibility can result in better bandgap tunability and wider infrared range making them more suitable for multi-junction integration (Parola et al., 2025; Sansom et al., 2021).

Although these materials have a lot of advantages, there are still many problems that these materials can't solve, this limits their efficiency and scalability. These include defect formation, compositional disorder, secondary phase formation, interface recombination, voltage deficits, which result in reduced lifetimes and device performance (ENNOUHI, 2025; Muhamad & Lafta, 2022).

In addition, III–V quaternary systems are still appealing for high efficiency tandem architectures, but they have more stringent requirements for compositional control in their fabrication and involve more material stability issues (Kret et al., 2021; Tournet et al., 2020).

Recent research also suggests that careful optimization of the subcell bandgaps, interfaceengineering and current matching is needed throughout all layers of the subcell to achieve successful design in a multijunction solar cell. Thus, the reliable, low-cost and efficient design of multijunction devices based on semiconductor alloys such as ternary and quaternary semiconductor alloys is one of the most significant challenges in the field of photovoltaics technology (Zhang et al., 2023; Amrillah et al., 2023).

III. METHODOLOGY

This work focusses on the study of the performance of $CuInTe_2$ and Cu_2ZnSnS_4 (CZTS) semiconductor alloys through an experimental thin film fabrication process and an analytical characterization method in the context of PV application. The method is to systematically make the devices and synthesize the materials and test their performance in controlled lab environments.

Glass substrates coated with FTO were used as transparent conducting electrode on which the The solar cell's structure was created. A chemical bath deposition (CBD) approach was utilized to create a CdS thin film as an n-type buffer layer to build a heterojunction with the absorber materials. The thin films' homogeneity, adhesion, and repeatability were made possible by the regulated chemical conditions under which the deposition process was conducted.
Two kinds of absorber layers, namely $CuInTe_2$ (ternary alloy) and CZTS (quaternary alloy) were produced by electrodeposition. The important deposition parameters including applied voltage, PH of electrolyte, concentration of precursors, deposition duration, etc. were tuned carefully to regulate the film growth, elemental composition, and crystalline integrity exactly.

Grain development and crystallinity were encouraged, structural flaws were decreased, and charge transfer was enhanced by further thermal annealing. In order to verify the films' phase purity and determine if any secondary phases were present, X-ray diffraction (XRD) and Raman spectroscopy were used.

A scanning electron microscope (SEM) coupled with an energy dispersive X-ray spectrometer (EDS) was used to analyze the surface morphology and elemental distribution. Moreover, ultraviolet visible spectroscopy was performed to evaluate optical spectrum and to compute values of bandgap. Current–voltage (J–V) measurements were used to assess the PV performance of the acquired devices under typical AM 1.5 illumination (100 mW/cm^2. Furthermore, capacitance-voltage (C–V) measurements were conducted to study the carrier concentration, dynamics of the depletion area and general properties of the junction. This methodological approach gives a strong platform to link the material synthesis, structural characteristics and photovoltaic performance, and hence to systematically assess the ternary and quaternary semiconductor alloys for solar cells applications.

IV. RESULTS

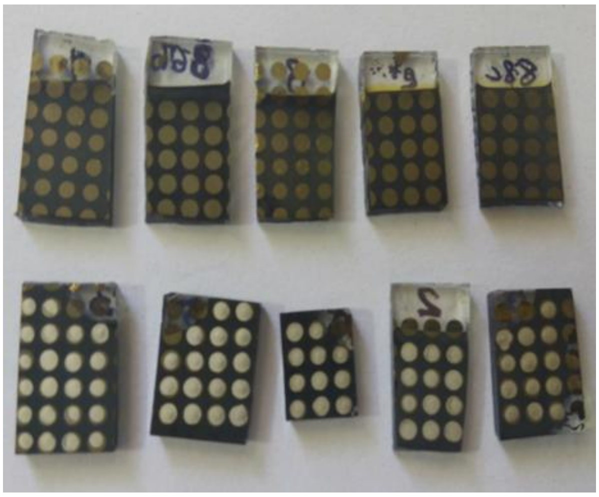
A significant number of studies have been performed that focus on chalcopyrite based solar cells on rigid and flexible substrates. In the case of CIGS solar cells having complex device structure, such as Mo back contact and antireflection coatings, a conversion efficiency of 21.7% has been reported (Jackson et al., 2016). Moreover, flexible polyimide substrates have shown efficiencies of 20.4%, which shows the need for sodium and potassium doping in the optimization process (Chirila et al., 2013). Some research works have been carried out by Molecular Beam Epitaxy (MBE) technique for CIT solar cell in the context of chalcopyrite family, which has been achieved the efficiency of 6.28% (Mise and Nakada, 2014). There is a critical report on the environmental friendly development of chalcogenide based thin film technologies on copper, which are not to be ignored in the latest comprehensive reviews (Amrillah et al., 2023; Muhamad and Lafta, 2022). While most commonly used for substrate designs, another means of creating thin film designs is to use a superstrate. The efficiency obtained for CIS solar cell grown by one-step electrodeposition by researchers is around 5%, with a p-i-n structure (Chaure et al., 2011). The potential for cost effective manufacturing processes has been shown in others reaching efficiencies of up to 4.5% in the growth of CIS with non-aqueous electrolytes (Londhe et al., 2018).

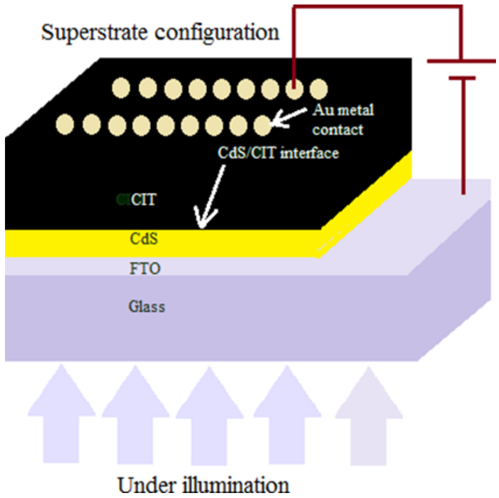
4.1 Device Fabrication Process

The FTO/CdS multilayer was coated with CIT to create the superstrate configuration solar cell. Before applying the CdS layers, the glass substrates coated with fluorine-doped tin oxide (FTO) were cleaned using double-distilled boiling water, acetone, and iso-propanol. They were then ultrasonically sonicated in iso-propanol for 15 minutes. High-quality environments at the interface and absence of defect formation in the following thin film structure may be produced by retaining the surface of substrate quality (Amrillah et al., 2023; Dalui et al., 2023). Chemical bath deposition was used to create the CdS layer on the FTO-coated glass substrates. After annealing at 450°C before the CIT layer was deposited, the CdS layer's thickness was determined to be between 70 and 80 nm. To guarantee ideal light transmission and minimize carrier recombination at the heterojunction interface, precise control over the window layer thickness and the post-deposition thermal treatment is essential (Anttu, 2023; Korotcenkov and Semikina, 2023).

4.1.1 Absorber Growth and Electrode

Contacts Cyclic voltammetry was applied to find –0.75 V as the best growth potential for the CIT absorber layer. The heterojunction was then deposited and then annealed at 450°C for 30 minutes in air to increase the crystallinity of the interface between CdS/CIT. Reducing structural flaws in the chalcogenide matrix depends on the electrochemical synthesis and thermal treatment conditions (Sansom et al., 2021; Tournet et al., 2020). Next, metal contacts containing both oxidizing and reducing chemicals were applied to the device's surfaces. The CIT layers were then followed by a layer of gold (Au) which was thermally evaporated at a base pressure of 10^{-6} mbar. As shown in Figure 1.1, this whole superstrate device design (FTO/CdS/CIT/Au) may serve as a solid foundation for an energy harvesting system with excellent efficiency.





CIT solar cells prepared by electrodeposition method

The superstrate architecture of the solar cell device is shown in figure 1.1, which is the FTO/CdS/CIT/Au device. The corresponding energy band diagram of CdS/CIT heterojunction is shown in figure 1.2

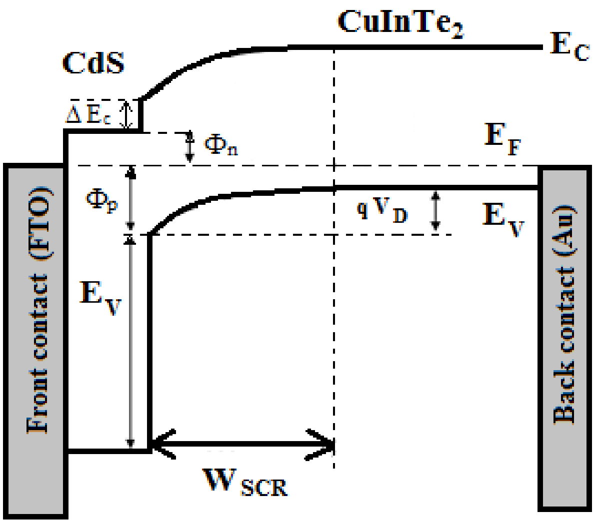
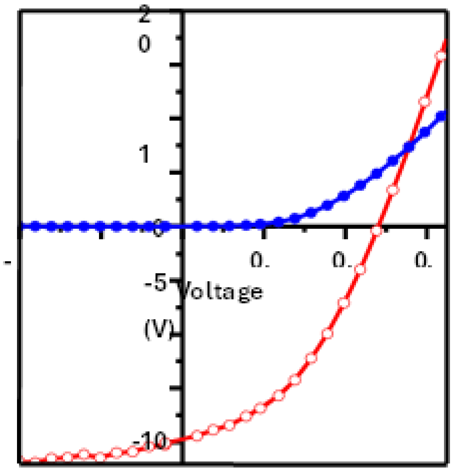


Figure 1.2 illustrates the corresponding energy band diagram for the CdS/CIT heterojunction

4.2 Current-Voltage (J-V) Characteristics

Figure 1.3 illustrates the sample dark and lighted current density-voltage (J-V) curves of the FTO/CdS/CIT/Au solar cell, which give critical information on the efficiency of the device and the underlying charge transport processes (Hu et al., 2024; Zidani et al., 2025). All optoelectronic experiments were conducted under AM 1.5 (100 mW cm^{-2}) conditions at a temperature of 25°C (Gonzalo Martín et al., 2021; Schygulla et al., 2020).



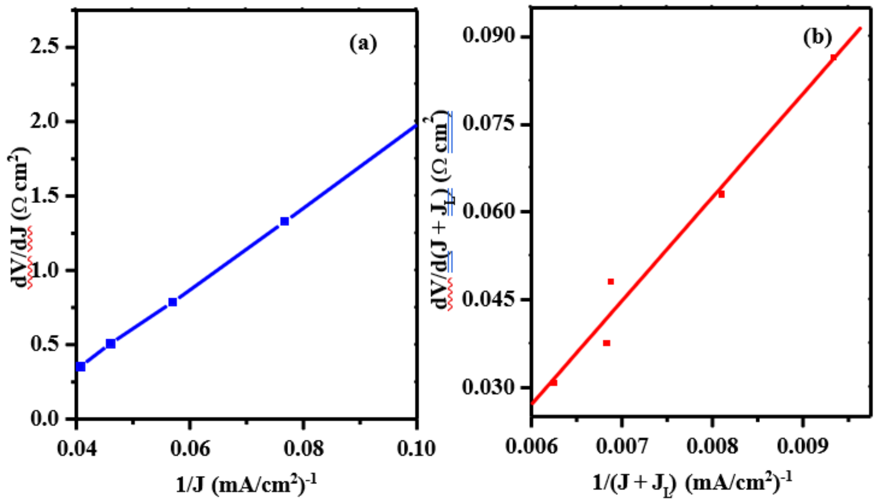
The representative dark and illuminated J-V performance curves of the FTO/CdS/CIT/Au solar cell have been plotted in Figure 1.3.

The device's open-circuit voltage (V_oc) is 480 mV, its fill factor (FF) is 43%, and its computed power conversion efficiency (η) is 4.13%. Its short-circuit current density (J_sc) is 20 mA/cm². It is observed that the ratio of Cu/In is critical for reaching optimum efficiency in Cu-In-Te thin-films (Hu et al., 2024; Zidani et al., 2025). In addition, the J-V data recorded under dark and light circumstances were examined by fitting them to the standard diode equations (Gonzalo Martín et al., 2021; Schygulla et al., 2020).

$$\frac{dV}{dJ} = \frac{Ak_BT}{q}\left(\frac{1}{J}\right) + R_s$$

$$\frac{dV}{d(J+J_L)} = \frac{Ak_BT}{q}\left(\frac{1}{J+J_L}\right) + R_s$$

The current density J is connected to the photocurrent density (J_L), applied voltage (V), ideality factor (A), series resistance (R_s), electronic charge (q), Boltzmann constant (k_B) and temperature (T). The following mathematical relations (Soley et al., 2024; Tournet et al., 2020) demonstrate how the values of the series resistance (R_s) and ideality factor (A) were derived from the y-intercepts (y) and slopes (S) of the plots given in Figure 1.4 (a) and (b), respectively:



The plots of (a) dV/dJ versus 1/J and (b) dV/d(J+J_L) versus 1/(J+J_L) for the solar cell device are shown under dark and illuminated conditions, respectively, as shown in figure 1.4.

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The series resistance (R_s) values were obtained as 334 Ω (dark) and 27 Ω (illuminated), which gave ideality factors of 1.43 and 1.63, respectively. The ideality factor is greater than 1, suggesting that the recombination and generation processes of the charge carriers are significant factors in the charge transport mechanism (Soley et al., 2024; Tournet et al., 2020).

4.3 Solar Cells Development at pH 4

The device architecture and fabrication processes were kept the same as before and solar cells were prepared with a deposition potential of –0.8 V and an electrolyte pH of 4.0 for CIT. In the guided way, these CIT layers were heat treated at a low temperature (80°C) in air ambient (Ennouhi, 2025; Zidani et al., 2025).

4.3.1 CIT Solar Cells Treated at 80°C for 30 and 60 Minutes

After adjusting the heat treatment at 80°C, the timeframes needed for constructing Cell A and Cell B were 30 minutes and 60 minutes, respectively. To improve the device efficiency and refine the absorber surface, the CdS/CIT layers were etched for one to two minutes in a sodium cyanide (NaCN) solution (Amrillah et al., 2023; Muhamad & Lafta, 2022). Following treatment, gold (Au) contacts with a thickness of 100–150 nm and an area of 0.05 cm² were thermally evaporated at a base pressure of 10^(-6) mbar. Schottky-type rectifying behavior is shown by the configuration FTO/CdS/CIT/Au (De Melo Cunha & Marques Lameirinhas, 2022; Parola et al., 2025). The potential barrier height (ϕ_b) in a dark situation was determined using the usual Richardson equation:

$$\phi_b = -\frac{k_B T}{q} \ln\left(\frac{A^{**}T^2}{J_s}\right)$$

Cell A and Cell B had computed potential barrier heights of 0.231 eV and 0.258 eV, respectively. The increase in barrier height with an increase in annealing time is thought to be caused by improved crystallinity and larger grain dimensions, whereas the decrease in reverse saturation current with the same increase in annealing time is thought to be caused by a decrease in grain boundary density (Dalui et al., 2023; Hidouri et al., 2021). At 0.3 V of the bias potential for Cell B, the rectification factor was around 10^2, and the diode current density was approximately 15 mA/cm². Figure 1.5 displays the AM 1.5 solar light current-voltage (J-V) characteristics of both devices (Hu et al., 2024; Korotcenkov & Semikina, 2023).

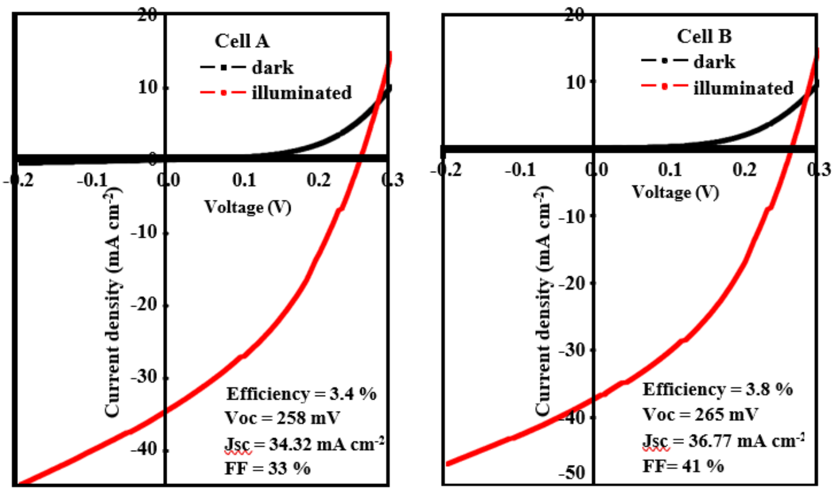


Figure 1.5 shows the typical dark and lighted J-V curves of the solar cells (FTO/CdS/CIT/Au) after 30-minute (Cell A) and 60-minute (Cell B) annealing.

Table 1.1 Solar cell characteristics of FTO/CdS/CIT/Au solar cells that were sequentially annealed for Cells A and B under light

Device	Annealing time	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (□) %
Cell A	30 minutes	258	34.32	33	3.4
Cell B	60 minutes	265	36.77	41	3.8

The power conversion efficiencies (η) of the produced CIT solar cells are about 3.4% and 3.8% on an area of 0.05 cm^2 for Cell A and Cell B respectively, which are reproducible. The crossover of the dark and illuminated J-V curves above the open-circuit voltage (V_oc) is probably due to the photoconductive response of the CdS window layer and the relatively low V_oc may result from recombination losses at the metal-semiconductor top interface (Hu et al., 2024; Zidani et al., 2025). Moreover, the low-temperature annealing process also leads to a small grain size, which leads to higher series resistance and carrier recombination (Dalui et al., 2023; Hidouri et al., 2021).

The series resistance (R_s) and ideality factor (n) were determined for both cells from the diode equations established above. The dark leakage currents of Cell A and Cell B were found to be 156 Ω and 140 Ω, respectively, with ideality factors of 4.13 and 3.33, respectively. These parameters were enhanced in illumination to R_s values of 47 Ω and 43 Ω for Cell A and Cell B, respectively, and ideality factors of 2.0 and 1.9 for Cell A and Cell B, respectively (Soley et al., 2024; Tournet et al., 2020). The current efficiency is good, yet the relatively low V_oc values indicate there is considerable scope for further improvements through optimization of the annealing temperatures, durations and surface treatment processes. Future studies could investigate ways to reduce the series resistance and improve the fill factor, thereby optimizing the overall performance of the device (Ennouhi, 2025; Muhamad and Lafta, 2022)..

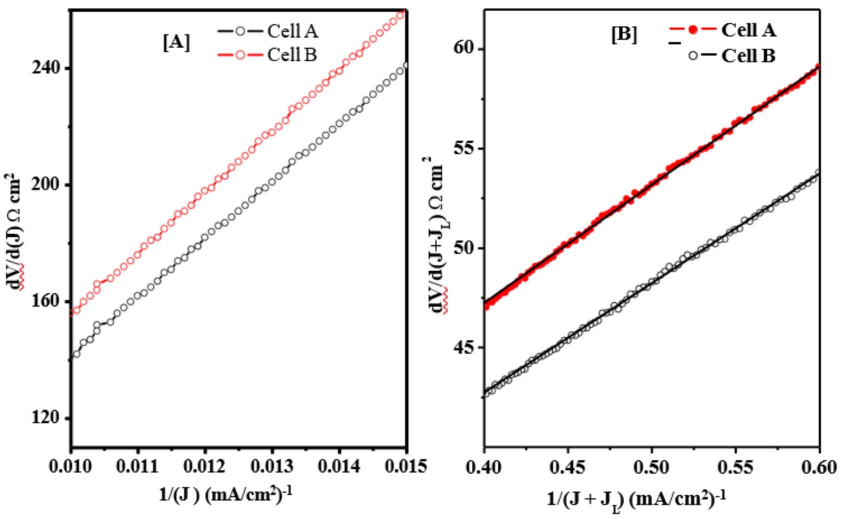


Figure1. 6 A plot of [A] dV/dJ verses 1/J under dark and [B] dV/d(J +J_L) versus 1/(J + J_L) of solar cell device under illuminated conditions for Cell A and Cell B, respectively

The capacitance-voltage (C-V) characteristics of both Cell A and Cell B were obtained at room temperature at a frequency of 100 kHz. The Mott-Schottky plots of 1/C^2 vs. bias voltage (V) of the FTO/CdS/CIT/Au solar cells after the successive high temperature treatment at 80°C under dark [A] and under illumination [B] conditions are shown in Figure 1.7. The Mott-Schottky plots show three distinct regions under dark conditions (Figure 1.7 [A]) and the x-axis intercept of the linear region (shown by the dashed line) yields the flat-band potential (Dalui et al., 2023; Korotcenkov and Semikina, 2023).

The concentration of the carriers (N_A) was determined as follows:

$$N_A = \frac{2}{q\epsilon_s}\left[-\left(\frac{d(1/C^2)}{dV}\right)\right]^{-1}$$

The N_A in this expression is the concentration of the acceptors, q is the electronic charge, ϵ_s is the permittivity of the semiconductor, and the term in the bracket on the right-hand side is the reciprocal of the slope of the 1/C^2 versus applied bias potential plot (Sansom et al., 2021; Tournet et al., 2020).

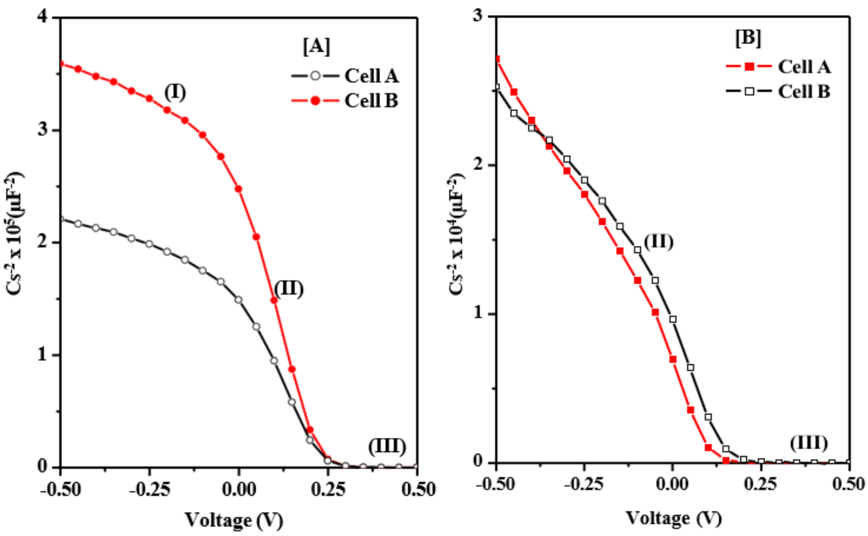


Figure 1.7 Mott-Schottky plots, $1/Cs^2$ versus bias voltage V for successively annealed FTO/CdS/CIT/Au solar cells at 80 °C under dark [A] and illumination [B] for Cell A and Cell B.

The Capacitance-Voltage (C-V) data were collected at 100 kHz, at room temperature, for both Cell A and Cell B. The Mott-Schottky plots of 1/C^2 vs. bias voltage (V) for the FTO/CdS/CIT/Au solar cells are shown in Figure 1.7 after successive heat-treatment in dark [A] and under illumination [B]. The carrier concentration of the cells were calculated as 2.0×10^20 cm^(-3) and 9.9×10^18 cm^(-3) for Cell A and B, respectively (Sansom et al., 2021; Tournet et al., 2020).

When illuminated (Figure 1.7 [B]) the devices remained depleted up to 0.2 V; above 0.25 V the devices showed a positive accumulation of carriers because of the diffusion of carriers. The capacitance-voltage (C-V) profile of the devices is shown in figure 1.8 with the total capacitance, C, increasing with the bias voltage. There are two components to the behavior in the junction: depletion capacitance (C_T) in the reverse bias region, due to the transition region dipole, and diffusion (storage) capacitance (C_D) in the forward bias region, due to charge storage effects. Interestingly, the values of C_D are higher than C_T and increase with the bias (Hu et al., 2024; Zidani et al., 2025).

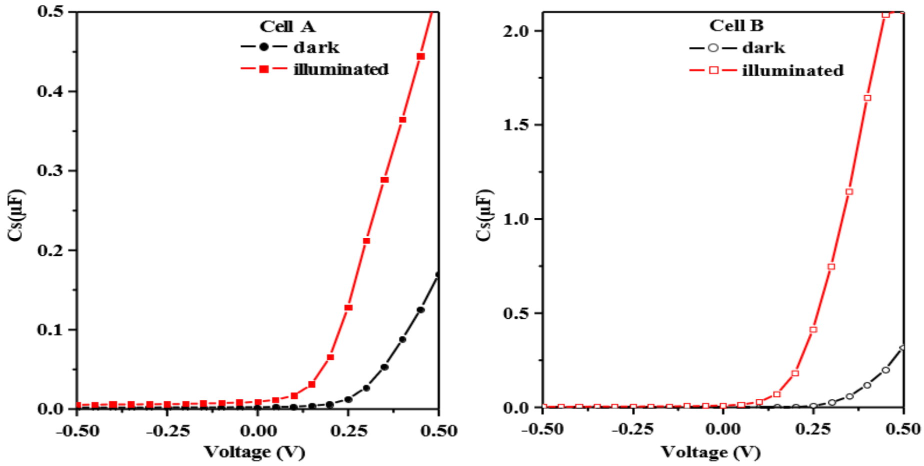


Figure 1.8 Capacitance-Voltage profile of the Cell A and Cell B under dark and illuminated condition

The samples were grown at -0.8 V (vs. Ag/AgCl) and yielded highly polycrystalline thin films of CIT that were then used to fabricate solar cells. The samples were etched in the 0.2 wt% NaCN solution for 90s before metal contact deposition. Dark and illuminated current density-voltage (J-V) characteristics (under 1.5 AM, 100 mW cm^{-2} illumination) were plotted as shown in Figure 1.9 (Amrillah et al., 2023; Muhamad and Lafta, 2022).

The short circuit current density (J_{SC}) of the device was 40.75 mA/cm^2, the open circuit voltage (V_{OC}) was 255 mV, the fill factor (FF) was 41%, and the power conversion efficiency (η) was 4.01%. The calculated barrier height (ϕ_b) was found to be 0.49 eV. The low V_{oc} is believed to be due to the high Cu/In ratio of 0.84 and the presence of recombination centers in the space charge region; this is a requirement for high efficiency CIT devices (typically, Cu/In ratio of 0.26–0.30 is required) (Hu et al., 2024; Zidani et al., 2025). To gain insight into the transport mechanisms, the series resistance (R_s) and ideality factor (n) are calculated using the standard diode equations, with the J_{sc} values near the J_{sc} (theoretical) limit set by the IR bandgap of CIT. (Soley et al., 2024; Tournet et al., 2020)

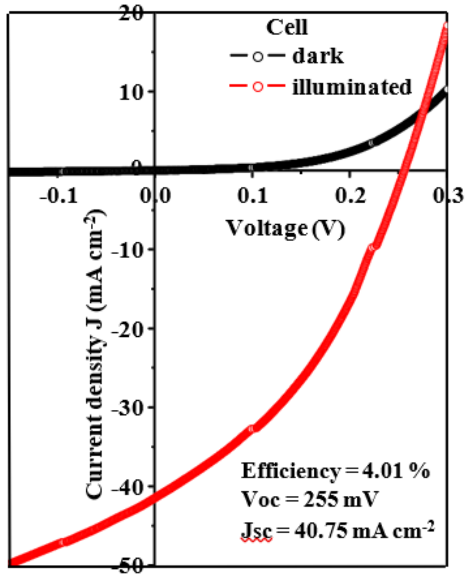
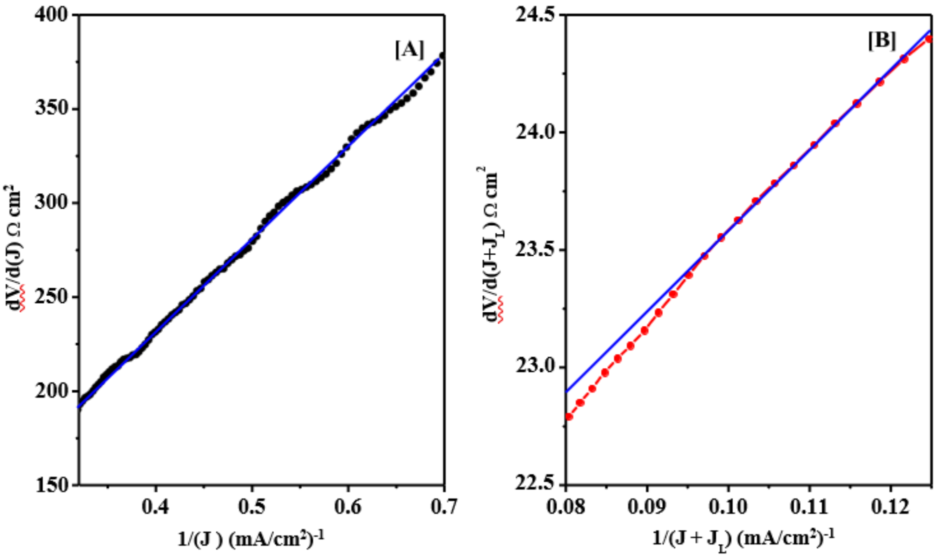


Figure 1.9 J-V characteristics measured for solar cell under dark and illuminated condition with light intensity 100 mW/cm^2 for FTO/CdS/CIT/Au solar cell structure

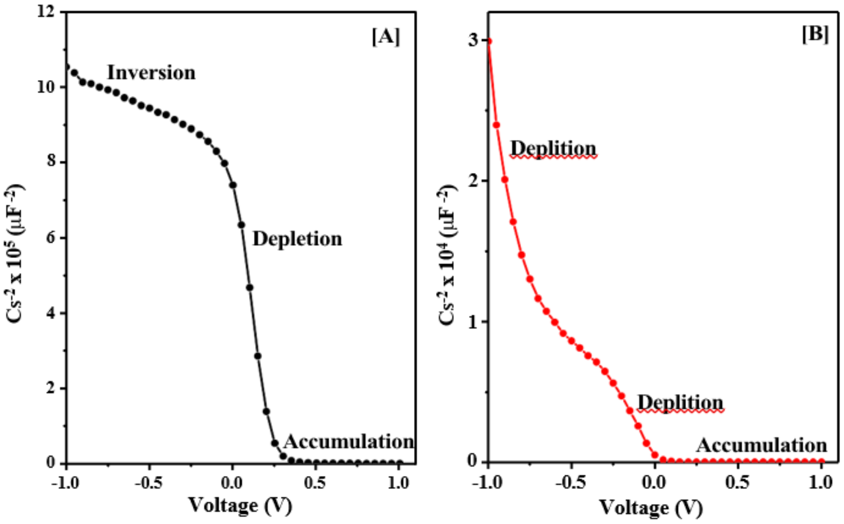
The plots of dV/dJ and dV/d(J+J_L) versus 1/J and 1/(J+J_L) respectively (Figure 1.10) were used to determine the values for series resistance (R_s) and ideality factor (n). These values were found to be 193 Ω and 4.84 under dark conditions, and 22.9 Ω and 3.21 under illuminated conditions (Soley et al., 2024; Tournet et al., 2020). These data show that the series resistance is quite high and non-ideal recombination is still present in the carrier transport regime. Further improvements in device performance can be obtained by the optimization of heat treatment temperatures, surface treatment after deposition and etching times (Ennouhi, 2025; Zidani et al., 2025) with high accuracy



The characteristic plots of (a) dV/dJ as a function of 1/J and (b) dV/d(J+J_L) as a function of 1/(J+J_L) of the solar cell device under dark and illuminated conditions, respectively, are shown in Figure 1.10.

The capacitance-voltage (C^(-2) versus V) characteristics of the solar cell were studied both in dark and illuminated conditions at a frequency of 100kHz as shown in Figure 1.11. The estimated drift/flat-band potential is about 260 mV in the dark state, and the Mott-Schottky plot shows three regions: inversion, depletion and accumulation (Sansom et al., 2021; Tournet et al., 2020). The carrier concentration obtained from equation (1.4) is about 1.4×10^19 〖" cm" 〗^(-3) at room temperature, which is in good agreement with Hall effect measurements as reported in V (Hu et al., 2024; Zidani et al., 2025).

Neither does it have a well-defined region of inversion when illuminated, but rather depletion over two ranges suggesting that the drift mechanism dominates under reverse bias. Once the charge carrier diffusion is initiated (at about 0.06 V), the sign of 'positive' indicates accumulation. The device stayed in accumulation mode when switched to the forward region, indicating that the diffusion mechanism is the dominant mechanism in the FORWARD region (Ennouhi, 2025; Muhamad and Lafta, 2022)..



A plot of 1/C^2 versus voltage (V) has been obtained for the solar cell device both in the dark (A) and under illumination (B) and is shown in Figure 1.11.

The concentration of the carriers in the illuminated material is about 2.9×10^21 〖" cm" 〗 ^(-3). This is attributed to the increase in carrier density mainly because of the photo-generation of charge carriers when illuminated.

V. Discussion

The present work shows that in heterojunction solar cells, the performance is greatly influenced by the ternary semiconductor $CuInTe_2$ and quaternary semiconductor Cu_2ZnSnS_4 (CZTS). The moderate power conversion efficiency of the $CuInTe_2$ based device (around 4.13%) was strongly dependent on the quality of the interfaces, defect density and carrier recombination process. The relatively low V_oc (480 mV) suggests the presence of recombination centers at the CdS/CIT interface and in the absorber layer. Moreover, an ideality factor value higher than one implies that recombination processes play a role in charge carrier transport. It is also revealed by series resistance measurements that the collection efficiency of the carriers is strongly affected by resistive losses.

Thermal annealing was found to be essential for improving device performance, due to the formation of superior crystallinity and grain growth, which led to decreased grain boundary defects and better charge transport. The barrier height observed after the annealing is increasing which indicates formation of a more stable junction with reduced leakage current. A comparative study of the optical and current generation properties shows that $CuInTe_2$ has good absorption but CZTS has more compositional flexibility and material sustainability. However, both materials are plagued by issues of compositional disorder, secondary phase formation and mismatch at interfaces. In conclusion, although ternary and quaternary alloys promise to be low-cost photovoltaic devices, additional research is needed to raise their efficiencies to those of more complicated III–V multi-junction devices.

VI. LIMITATIONS

The study is conducted at laboratory scale thin film solar cell fabrication and hence it is not an indicator of the large area industrial scale up.

Unfortunately, the efficiency (~4.13%) is not the best for III–V multijunction solar cell. The study does not include any studies of long term stability under real environmental conditions as this would be needed for commercial applications.

Besides this, a strict control of the stoichiometry in the film is still not easy to achieve, which results in different film qualities and device reproducibility.

The other disadvantage was the defect at the CdS/absorber junction that could not be completely removed by the present annealing and surface treatment conditions. The advanced passivation techniques were not investigated in this work..

VII. CONCLUSION

The results of this research highlight the importance of ternary $CuInTe_2$ and quaternary Cu_2ZnSnS_4 (CZTS) semiconductor alloys for multi-junction PV application. The fabricated $CuInTe_2$ heterojunction solar cell also demonstrated a maximum power conversion efficiency of 4.13%, indicating the possibility of using the electrodeposited thin films in solar energy harvesting applications. The availability and versatility of composition seem to be the advantages of quaternary alloys while the optical absorption and photocurrent generation properties appear to be the advantages of ternary alloys. Thus, improvement of annealing processes, further development of the interface engineering, and defect passivation process are crucial to maximize the device performance. To conclude, these ternary and quaternary alloys are good candidates for the second generation PV technologies based on economics, but need further advancement to achieve the full potential of high efficiency multi-junction PV technologies.

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